S.E Sem III CBGS (ETRX)

DCD :

3/12/2015

QP Code : **5159**

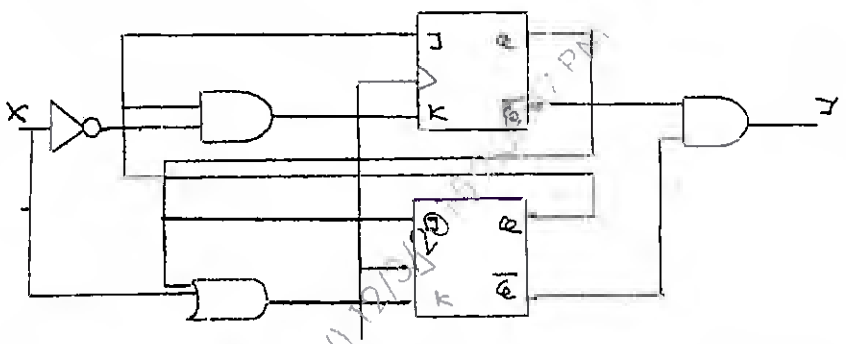
(3 Hours) [Total Marks : 80

N. B. : (1) Question No. 1 is compulsory.
(2) Attempt any three out of the remaining four questions.
(3) Use suitable data, wherever necessary.

1. (a) Explain drawback of synchronous counter. 5
(b) Differentiate synchronous and asynchronous counter. 5
(c) Draw truth table and logical diagram of half adder. 5
(d) Explain Fan in, fan out, power dissipation and noise immunity with reference to digital ICs 5

2. (a) Design MOD 12 asynchronous counter using T flip flop. 10
(b) Discuss Xilinx XC 9500 CPLD architecture. 10

3. (a) Design MOD-60 counter using IC 74163. 10
(b) Analyze the sequential state machine shown in figure. Obtain state diagram for the same 10



4. (a) Simplify following logic function and realize using NAND gates 10
(i) F=1:m(1,2,4,7, 10,11,13)+d(9,15)
(ii) F=2:m(1,2,3,5,8,9,11,13,15) + d(6)
(b) Design a Mealy type sequence detector to detect a serial input sequence of 101. 10

5. (a) Draw a circuit diagram of two input TTL NAND gate and explain its operation. 10
(b) Design 4 bit Johnson counter using J-K Flip Flop. Explain it operation using waveform. 10

6. Write a short note on 20
(a) Fault Model.
(b) Multiplexers.
(c) Noise Margin.

MD-Con. 9616-15.